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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/022,428	12/20/2001	Yusuke Matsushima	NEC01P202	5194

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EXAMINER	
TABONE JR, JOHN J	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 05/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/022,428	MATSUSHIMA, YUSUKE	
	Examiner	Art Unit	
	John J Tabone, Jr.	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3 & 4*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-6 have been examined.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-3, and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by Zasio et al. (US-4495629).

Claims 1:

Zasio teaches a D flip-flop with a master section of the latch, comprising of transmission gates T1 and T2 and inverters I1, and I2, and the slave section comprising of transmission gates T3 and T4 and inverters I3 and I4 which operate under the control of the clock signal C. Zasio includes transmission gate T3 in the slave section as the clock controller which receives input from the master section (master latch) and outputs the data signal to the slave section (slave latch) during normal mode of operation. Zasio further teaches a transmission gates T7 (second scan controller) that is used to control the scan data to the SO output of I5 during scan mode. Zasio discloses that the separate transmission gates T7 (second scan controller) is used as not to load down the clock controller during normal mode. (Col. 4, lines 31-52; col.6, lines 19-32; Fig. 3). The

inclusion of a first scan controller is merely a design choice and does not, by any means, effect the operation of the master-slave latch during either normal or scan operation. A person of ordinary skill in the art could appropriately design this as the design demands. During scan mode the first scan controller 5 is transparent and does not effect normal operation. The alleged improvement to the prior art by the instance application is to create a faster master-slave flip-flop by off-loading the clock controller from driving the scan controller section during normal mode (page 12, lines 21-24). Zasio teaches all these elements.

Claim 2:

Zasio teaches a D flip-flop in Fig. 3.

Claims 3 and 5:

Zasio teaches a D flip-flop with a master section of the latch, comprising of transmission gates T1 and T2 and inverters I1, and I2, and the slave section comprising of transmission gates T3 and T4 and inverters I3 and I4 which operate under the control of the clock signal C. Zasio includes transmission gate T3 in the slave section as the clock controller which receives input from the master section (master latch) and outputs the data signal to the slave section (slave latch) during normal mode of operation. Zasio further teaches a transmission gates T7 (second scan controller) that is used to control the scan data to the SO output of I5 during scan mode. Zasio discloses that the separate transmission gates T7 (scan controller) is used as not to load down the clock controller during normal mode. (Col. 4, lines 31-52; col.6, lines 19-32; Fig. 3).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 4 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zasio et al. (US-4495629).

Claims 4, and 6:

Zasio does not explicitly disclose a J-K and T scan flip-flops, however Zasio does teach a D scan flip-flop. It would have been obvious to one of ordinary skill in the art at the time the invention was made to adapt the design of off-loading the clock controller of a J-K or a T flip-flop for use of scan testing as Zasio' s D flip-flop. The artisan would have been motivated to do so because it would allow for faster flip-flop operation during normal mode.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Gaudet et al. (US-5633606)

Gaudet teaches SCAN flip-flop with a master latch 204 which drives a clock controller 210 connected to a slave latch 206. Gaudet also teaches the master latch 204 drives a scan controller 212 in a scan output section 208.

Kanji Hirabayashi (JP-63253272)

Hirabayashi teaches SCAN flip-flop with a master latch which drives a clock controller connected to a slave latch. Gaudet also teaches the master latch drives a scan controller in a scan output section.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J Tabone, Jr. whose telephone number is (703) 305-8915. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JJT

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